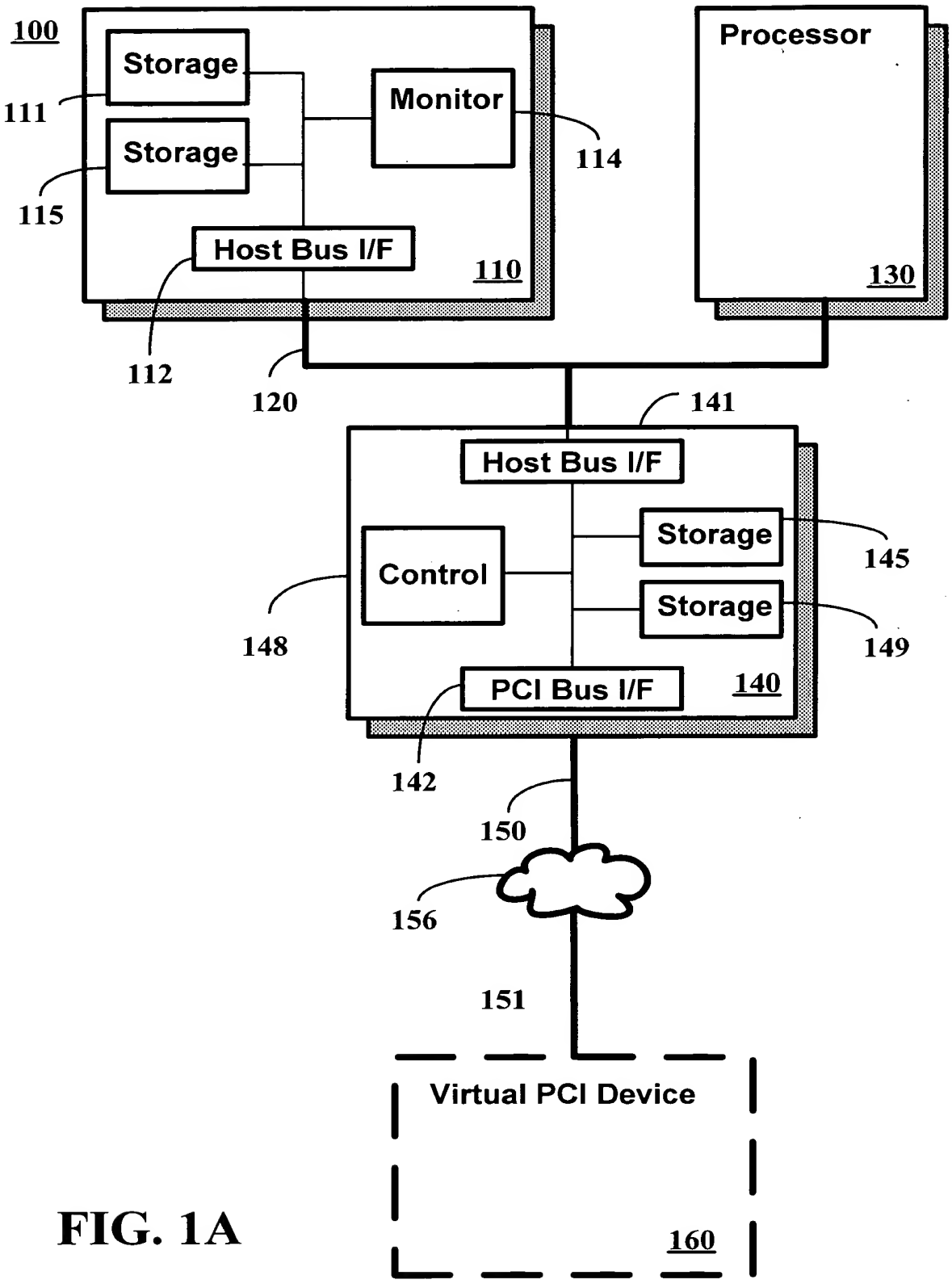

100
Storage
111
Storage
115
Monitor
114
Host Bus I/F
110
112
120
Processor
130
141
Host Bus I/F
Storage
145
Control
148
Storage
149
PCI Bus I/F
140
142
150
156
151
Virtual PCI Device
160

FIG. 1A

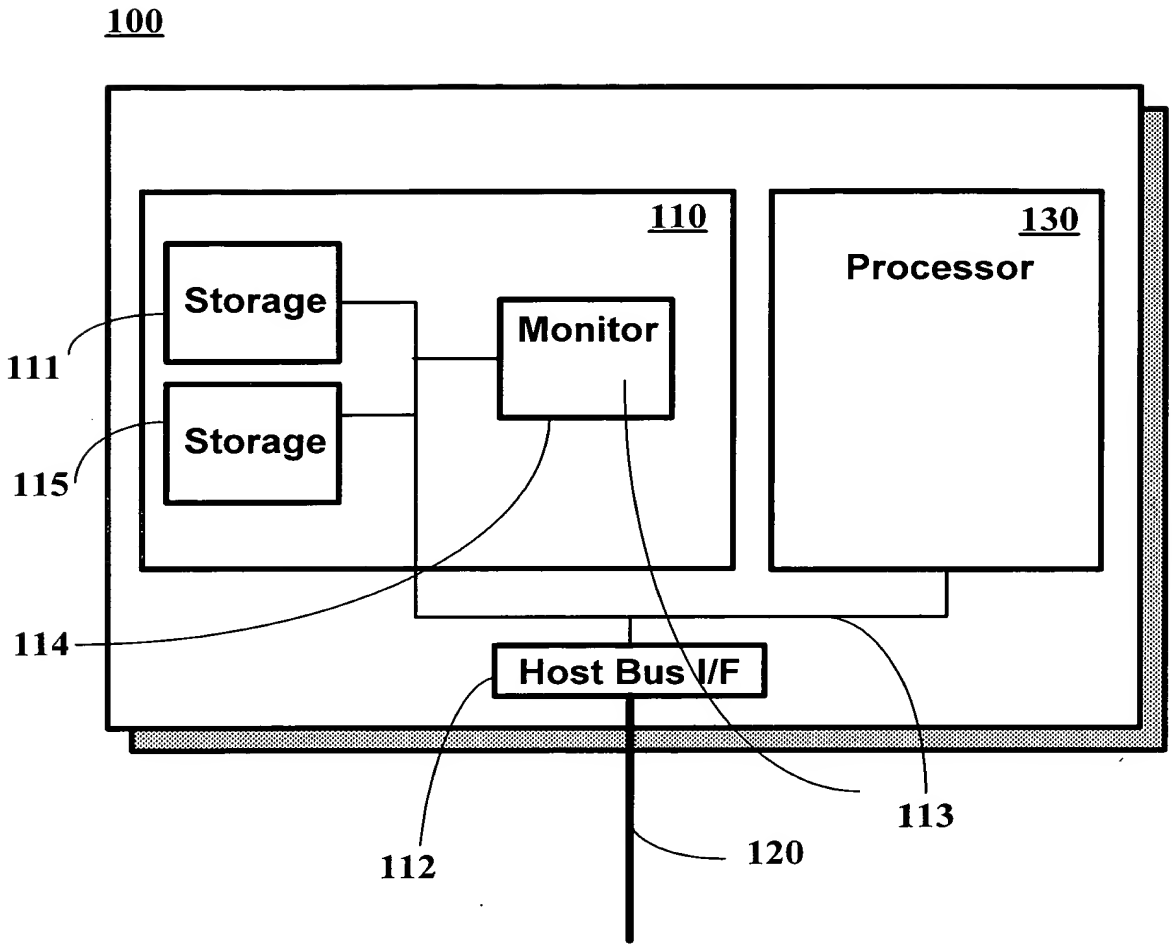

100
110
130
Processor
Storage
Storage
Monitor
111
115
114
Host Bus I/F
112
113
120

FIG. 1B

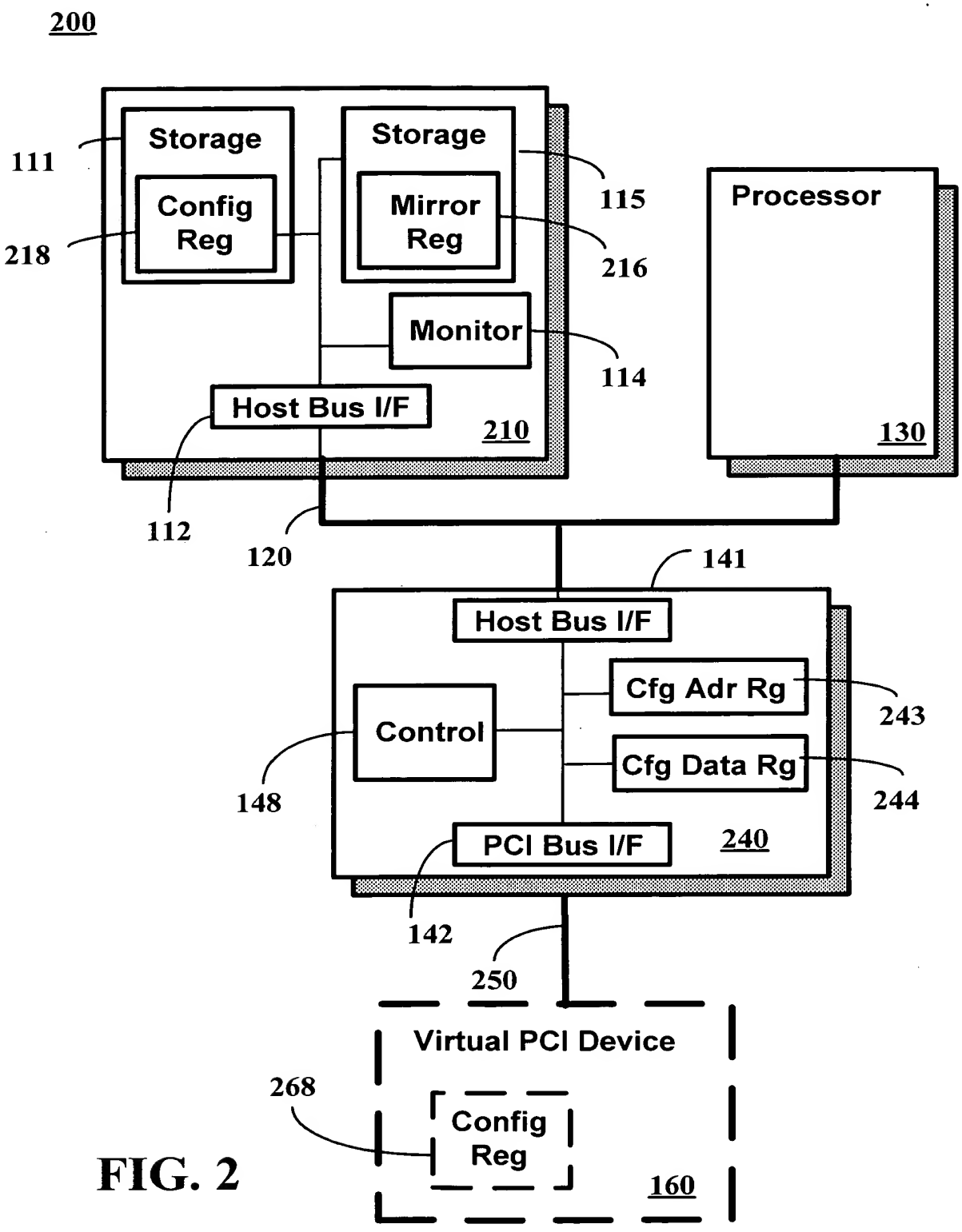

200
Storage
Config Reg
Storage
Mirror Reg
Monitor
Host Bus I/F
210
Processor
130
111
218
115
216
114
112
120
141
Host Bus I/F
Cfg Adr Rg
Cfg Data Rg
Control
PCI Bus I/F
240
243
244
148
142
250
Virtual PCI Device
268
Config Reg
160

FIG. 2

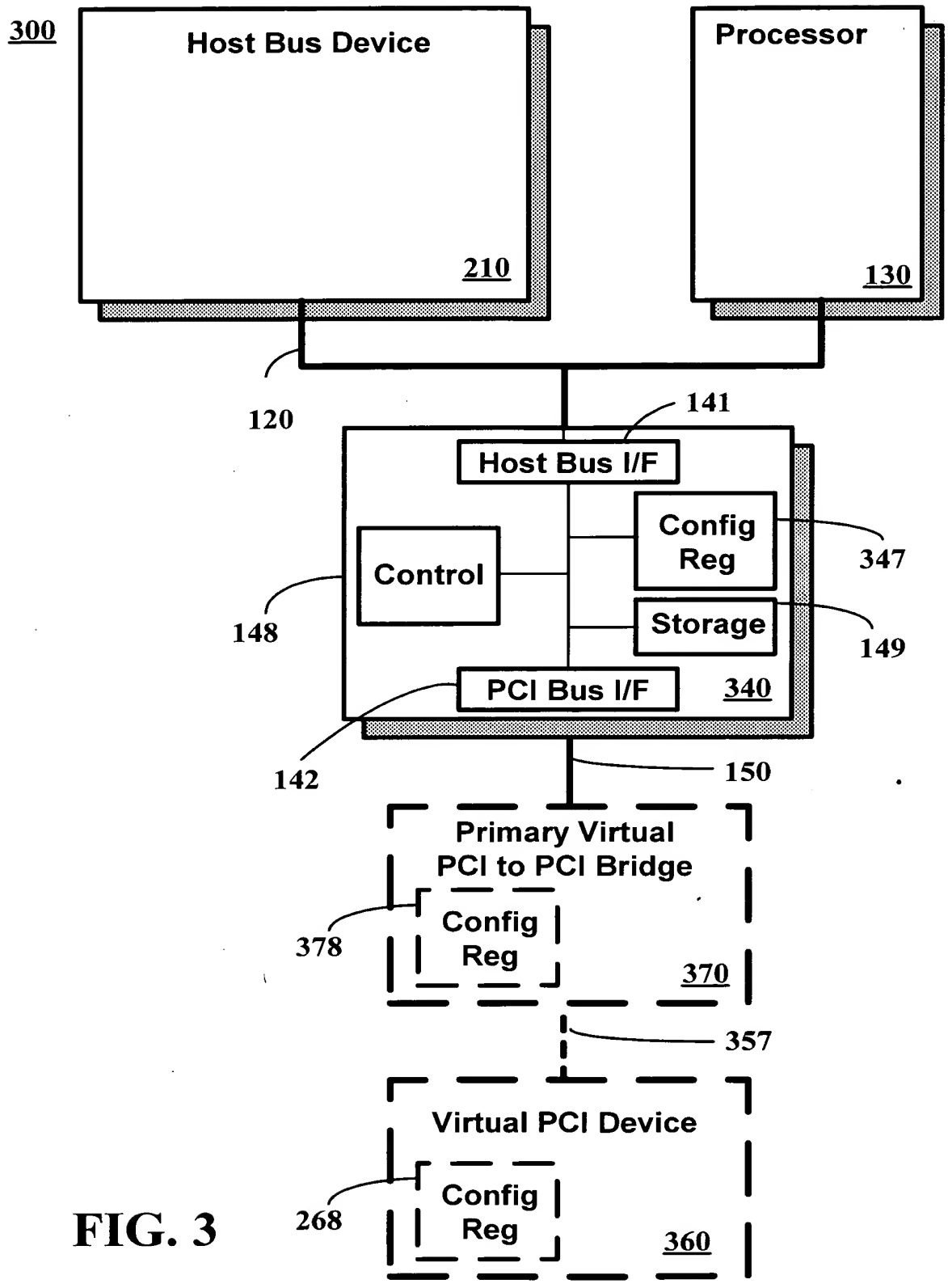

300
Host Bus Device
210
Processor
130
120
141
Host Bus I/F
Config Reg
347
Control
148
Storage
149
PCI Bus I/F
340
142
150
Primary Virtual PCI to PCI Bridge
Config Reg
378
370
357
Virtual PCI Device
Config Reg
268
360

FIG. 3

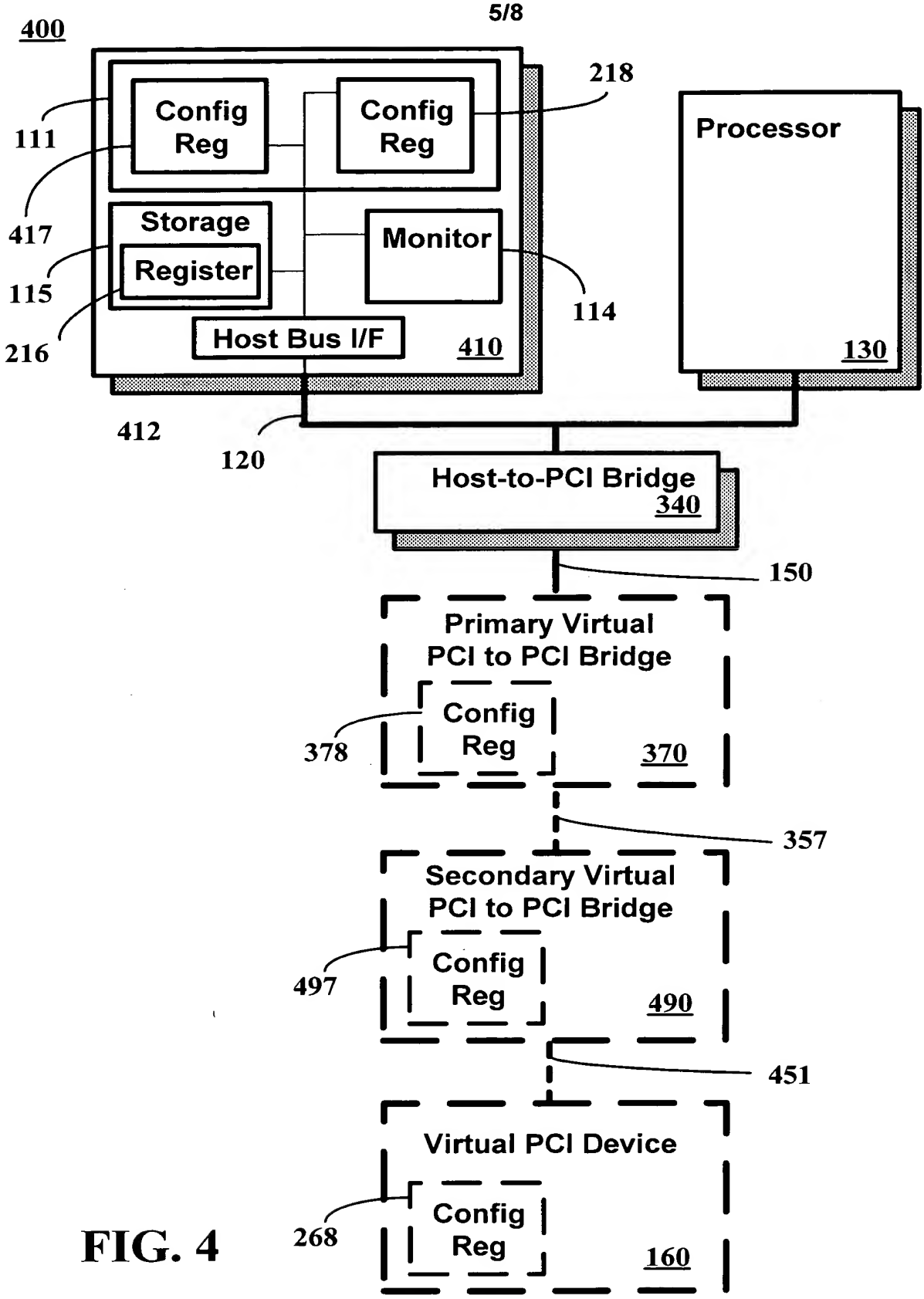

400
Config Reg
Config Reg
218
111
417
Storage
Register
Monitor
115
114
216
Host Bus I/F
410
Processor
130
412
120
Host-to-PCI Bridge
340
150
Primary Virtual PCI to PCI Bridge
Config Reg
378
370
357
Secondary Virtual PCI to PCI Bridge
Config Reg
497
490
451
Virtual PCI Device
Config Reg
268
160

FIG. 4

FIG. 5

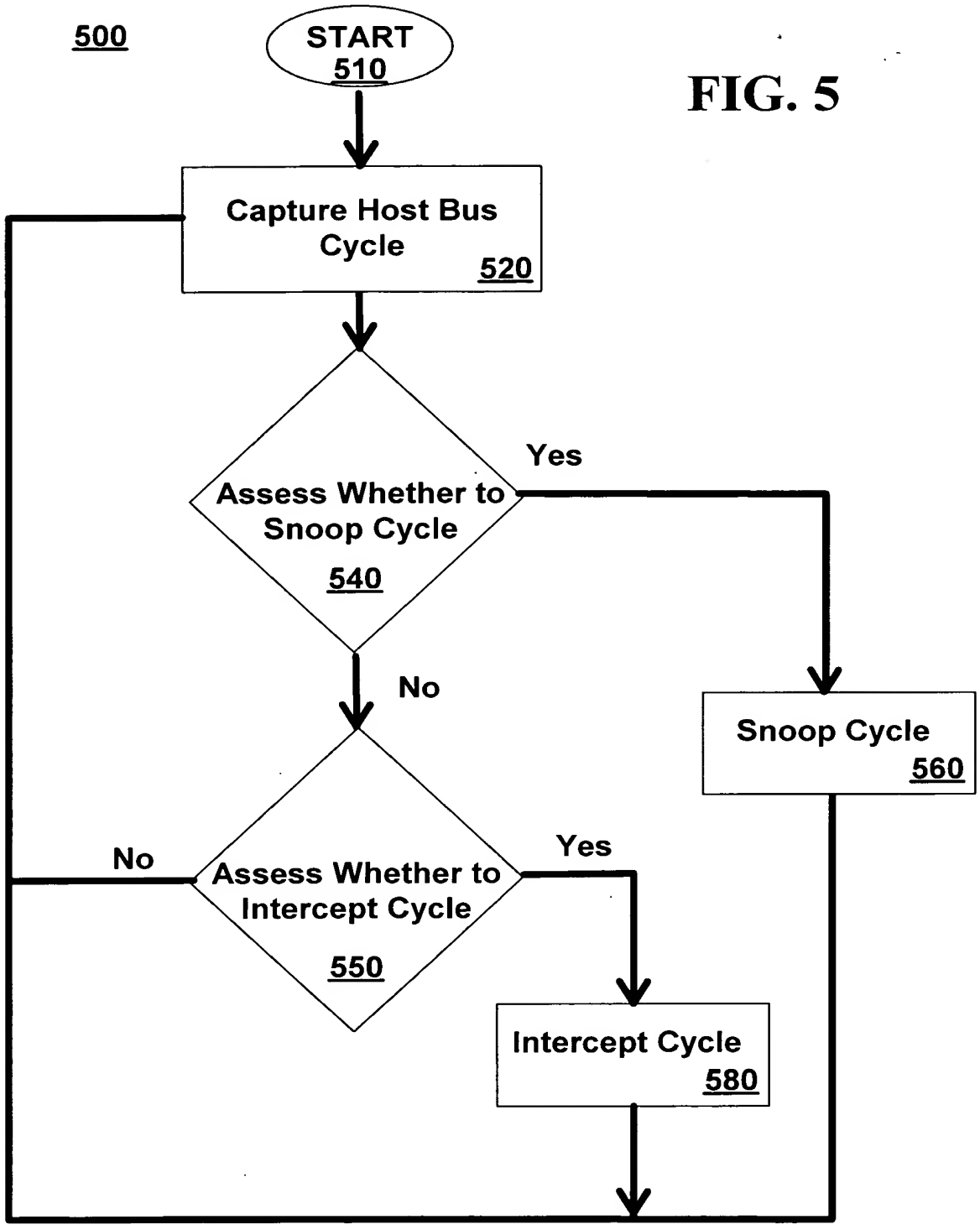
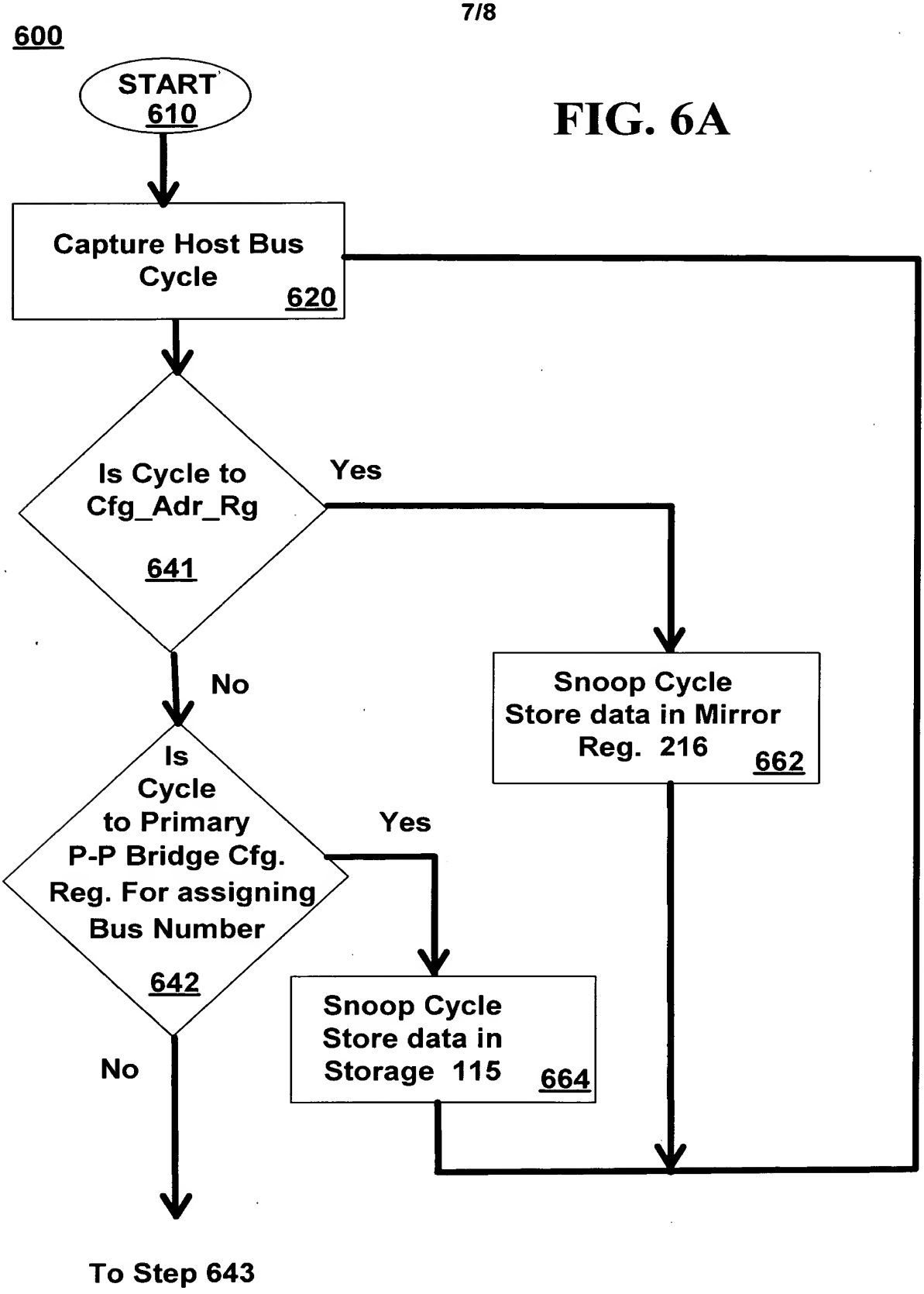

500
START
510
Capture Host Bus Cycle
520
Assess Whether to Snoop Cycle
540
Yes
No
Snoop Cycle
560
Assess Whether to Intercept Cycle
550
No
Yes
Intercept Cycle
580

FIG. 6A


600
START
610
Capture Host Bus Cycle
620
Is Cycle to Cfg_Adr_Rg
641
Yes
No
Snoop Cycle Store data in Mirror Reg. 216
662
Is Cycle to Primary P-P Bridge Cfg. Reg. For assigning Bus Number
642
Yes
No
Snoop Cycle Store data in Storage 115
664
To Step 643

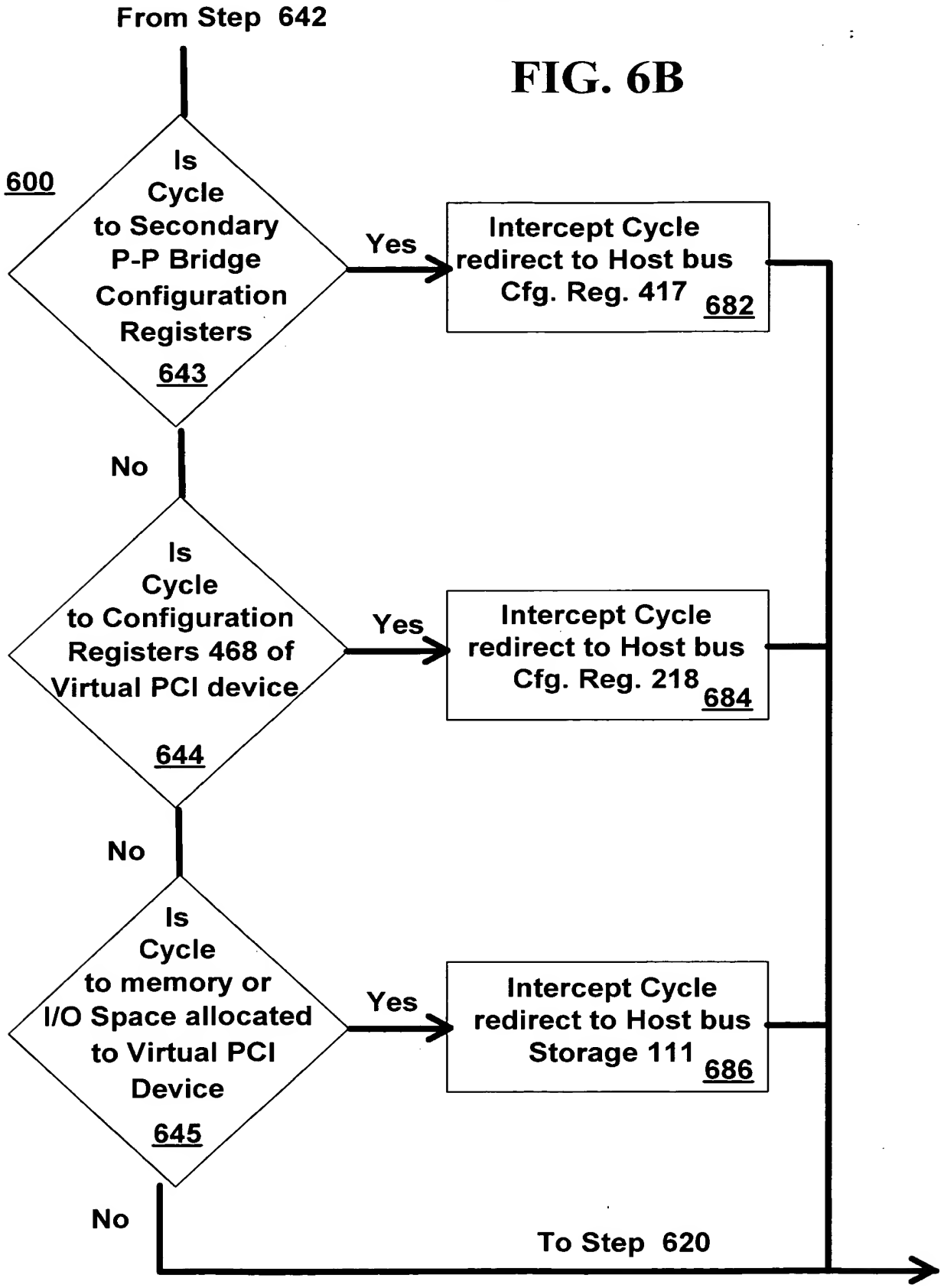

From Step 642
600
Is Cycle to Secondary P-P Bridge Configuration Registers 643
Yes
Intercept Cycle redirect to Host bus Cfg. Reg. 417 682
No
Is Cycle to Configuration Registers 468 of Virtual PCI device 644
Yes
Intercept Cycle redirect to Host bus Cfg. Reg. 218 684
No
Is Cycle to memory or I/O Space allocated to Virtual PCI Device 645
Yes
Intercept Cycle redirect to Host bus Storage 111 686
No
To Step 620

FIG. 6B